



SEMICONDUCTOR MEMORY ELEMENT ARRANGEMENT

CROSS-REFERENCE TO RELATED APPLICATION

This application is a continuation of International Patent Application Serial No. PCT/DE02/02742, filed July 25, 2002, which published in German on April 3, 2003 as WO 03/028107, and is incorporated herein by reference in its entirety.

FIELD OF THE INVENTION

The invention relates to a method for fabricating a semiconductor memory element arrangement, a method for operating a semiconductor memory element arrangement and a semiconductor memory element arrangement.

BACKGROUND OF THE INVENTION

Essential parameters of a semiconductor memory element arrangement are the retention time for which the memory content stored in the individual semiconductor memory elements is preserved, the write time required for programming in the memory content, and the write voltages required for programming in the memory content.

A known semiconductor memory element is the RAM memory element (RAM = Random Access Memory) which, although having relatively fast write times of a few nanoseconds, has only short retention times on account of unavoidable leakage currents, so that the RAM memory element has to be recharged at regular time intervals of about 100 ms.

By contrast, although the so-called EPROM memory element (EPROM = Electrically Programmable Read Only Memory) enables relatively long retention times of a